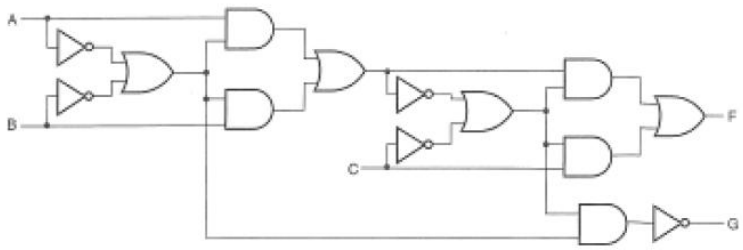
Κατ' όικον Εργασία 3

1. Draw the multi-level NAND logic diagram for each of the following expressions:

    a. W(X+Y+Z) + XYZ
    b. (A'B+CD')E + BD'(A+B)

2. Convert the following logic diagram to:

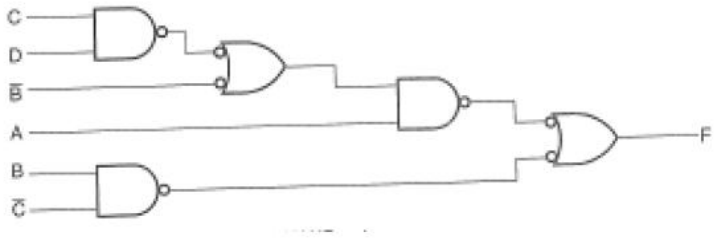
    a. An all-NAND diagram
    b. An all-NOR diagram



3. Draw the necessary XOR/XNOR circuits for a 3-bit parity generator and 4-bit parity checker, using even parity bit.

4. Let tpd be defined as the average of tPHL and tPLH. Calculate the delay between each input and output in the logic circuit below, by:

    a. Calculating tPHL and tPLH for each path, assuming tPHL=1ns and tPLH=2ns for each gate and averaging the path delay to find tpd.
    b. Using tpd=1.5ns for every gate.
    c. Compare your answers in ***(a)*** and ***(b)*** and discuss any differences.

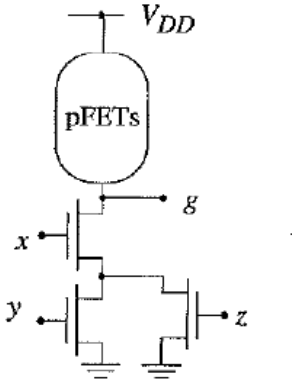


5.

    a. Connect the outputs of three tri-state buffers together, and add additional logic to implement the function F = A'BC + ABD + AB'D'. Assume that signals C, D, and D' are data inputs to the buffers and signals A and B pass through logic that generates the enable inputs.
    b. Is your design in part ***(a)*** free of tri-state output conflicts? If not, change the design to be free of such conflicts.

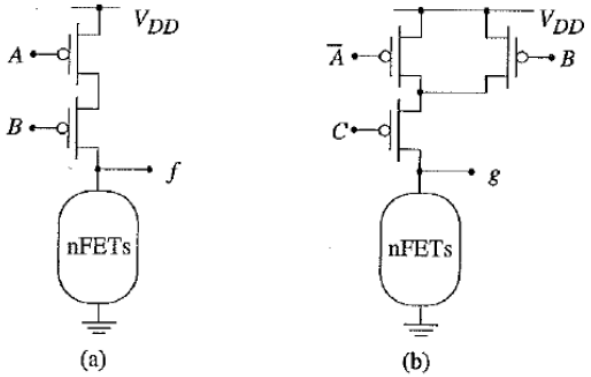
6. The CMOS logic gate below shows only the nMOS (pull-down) network.

    a. Determine the function g(x,y,z) and construct its truth table
    b. Complete the CMOS logic diagram by designing the pMOS (pull-up) network.



7. The CMOS logic gates below show only the pMOS (pull-up) network.

    a. Determine the function at each gate
    b. Complete the CMOS logic diagrams by designing the nMOS (pull-down) networks.



8. Draw the CMOS logic diagram, with a minimum number of transistors, for function g=((x+y)z+w)':

    a. Using only CMOS basic gates
    b. Using a single CMOS complex gate