

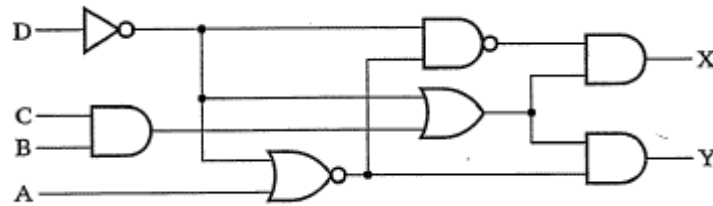


## Κατ' όικον Εργασία 5

- Consider unsigned binary numbers and perform the following subtractions by taking the 2s complement of the subtrahend:  
(a)  $11010 - 10001$   
(b)  $11110 - 1110$   
(c)  $1111110 - 1111110$   
(d)  $101001 - 101$
- The following binary numbers have a sign in the leftmost position and, if negative, are in 2s complement form. Perform the indicated arithmetic operations and verify the answers:  
(a)  $100111 + 111001$   
(b)  $001011 + 100110$   
(c)  $110001 - 010010$   
(d)  $101110 - 110111$
- Find the 9's complement of the following 8-digit decimal numbers:  
(a) 21569741  
(b) 01010100  
(c) 90419910  
(d) 00000000
- Design a 5-bit signed-magnitude adder-subtractor. Divide the circuit into 3 parts: (a) sign generation and add-subtract control logic, (b) an unsigned number adder-subtractor using 2s complement of the minuend for subtraction, and (c) selective 2s complement result corrections logic.
- Design simplified (minimum, in terms of hardware cost) circuits for (a) and (b) below. In each case, you can assume that the input combinations not corresponding to decimal digits give don't care outputs.  
(a) A circuit that generates the 9's complement of a BCD digit  
(b) A circuit that generates the 9's complement of an excess-3 digit
- Design a BCD adder-subtractor using the BCD adder discussed in class and the 9's complementer from problem 5(a), as well as other logic or functional blocks, as necessary. Use block diagrams for the components, showing only inputs and outputs where possible.
- Consider an 8-bit binary multiplier with inputs  $X = x_7x_6x_5\dots x_1x_0$  and  $Y = y_7y_6y_5\dots y_1y_0$  and output  $P = p_{15}p_{14}p_{13}\dots p_1p_0$ . Give the diagram of the multiplier using the 2-input AND gate and the 1-bit FA as the only basic building blocks. How many such blocks do you need? (express it with respect to the inputs of the circuit) Also, what is the maximum propagation delay? (express it with respect to the delay of the basic building blocks).
- Write a structural VHDL description of the circuit shown below. Compile and simulate your code for all possible input combinations to verify the



correctness of your description.\*



9. Write a dataflow VHDL description for the circuit of Problem 8. Again, compile and simulate your code for all possible input combinations to verify the correctness of your description.\*
10. Write a VHDL description for a 4-to-2 priority encoder, using the “when-else” statement. Compile and simulate your code for a set of input combinations that are a good test for the circuit.\*
11. Write a VHDL description for an 8-to-1 multiplexer using the “with-select” statement. Compile and simulate your code for a set of input combinations that are a good test for the circuit.\*

*\* For all the VHDL problems, you must submit your simulation results (functional waveforms).*