Κατ' όικον Εργασία 6

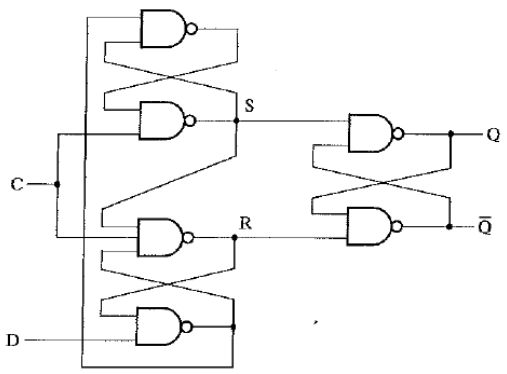
1. Perform a manual of computer-based logic simulation for the *S'R'* latch (similar to the one discussed in class for the *SR* latch). Construct the input sequence, keeping in mind that changes in state for this type of latch occur in response to 0 rather than 1.

2. Perform a manual of computer-based logic simulation for the *SR* latch with control input *C* (similar to problem 1). In particular, examine the behavior of the circuit when *S* and *R* are changed while *C* has the value 1.

3. Obtain the logic diagram of a *D* latch with control input *C*, using NOR/NOT gates only (instead of NAND/NOT gates, as discussed in class).

4. Obtain the logic diagram of the *SR* master-slave flip-flop, using NAND/NOT gates only.

5. A popular alternative design for a positive-edge-triggered *D* flip-flop is shown below. Manually or automatically simulate the circuit to determine whether its functional behavior is identical to that of the alternative design discussed in class.



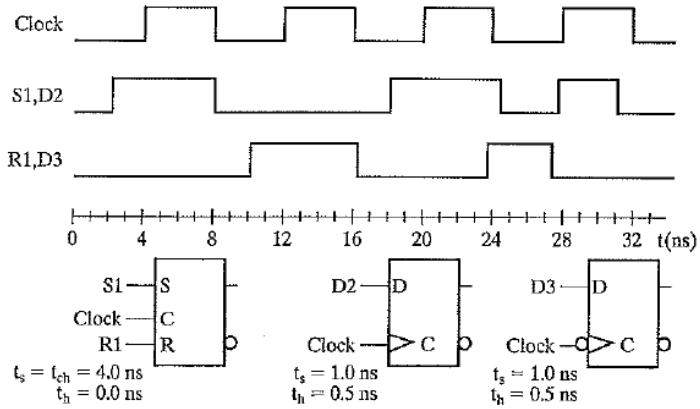
6. Obtain a timing diagram for a *JK* master-slave flip-flop during four clock pulses (similar to the one for an *SR* master-slave flip-flop given in your textbook). Show the timing signals for *C, J, K, Y,* and *Q*. Assume that initially the output *Q* is equal to 1, with the first pulse *J=0* and *K=1*. Then, for successive pulses, *J* goes to 1, followed by *K* going to 0 and then *J* goes back to 0. Assume that each input changes after the negative edge of the pulse.

7. Repeat Problem 6, using a positive-edge-triggered *JK* flip-flop. Show the timing diagrams for *C, J, K*, and *Q*.

8. Write *characteristic equations* for each type of flip-flop (*SR, JK, D*, and *T*). A characteristic equation gives the function *Q(t+1)* in terms of *Q(t)* and the input variables to the flip-flop.

9. A set of waveforms applied to *SR* and *D* flip-flops is shown below. These waveforms are applied to the flip-flops shown along with the values of their timing parameters.
(a) Indicate the locations on the waveforms at which there are input combinations or timing parameter violations in signal *S1* for flip-flop 1.
(b) Indicate the locations on the waveforms at which there are input combinations or timing parameter violations in signal *R1* for flip-flop 1.
(c) List the times at which there are timing parameter violations in signal *D2* for flip-flop 2.
(d) List the times at which there are timing parameter violations in signal *D3* for flip-flop 3.

Violations should be indicated even if the state of the flip-flop is such athat the violations will not affect the next state.



10. A sequential circuit with two *D* flip-flops *A* and *B*, two inputs *X* and *Y*, and one output *Z* is specified by the following input equations:

$$D_A = X'A + XY \qquad D_B = X'A + XB \qquad Z = XB$$

(a) Draw the logic diagram of the circuit.
(b) Derive the state table.

11. A sequential circuit has one flip-flop *Q*, two inputs *X* and *Y*, and one output *S*. The circuit consists of a *D* flip-flop with *S* as its output and logic implementing the function:

$$D = X \oplus Y \oplus S$$

with *D* as the input to the *D* flip-flop. Derive the state table of the sequential circuit.