Κατ' όικον Εργασία 8

1. Design the basic cell of a universal shift register to the following specifications. The internal storage elements will be positive edge-triggered D flip-flips. Besides the clock, the shifter stage has 2 external control signals, S_0 and S_1, and 3 external data inputs, SR, SL, and DI. SR is the input data being shifted into the cell from the right, SL is data being shifted from the left, and DI is parallel load data. The current value of the flip-flop will be replaced according to the following settings of the control signals: $S_0 = S_1 = 0$: replace D with DI; $S_0 = 0$ and $S_1 = 1$: replace D with SL; $S_0 = 1$ and $S_1 = 0$: replace D with SR; $S_0 = S_1 = 1$: hold the current state. Draw a schematic for this basic shifter cell.

2. Draw the logic diagram of a 4-bit register with mode selection inputs S_0 and S_1. The register is operated according to the following: $S_0 = S_1 = 0$: hold the current state; $S_1 = 0$ and $S_0 = 1$: complement output; ; $S_1 = 1$ and $S_0 = 0$: load parallel data; ; $S_0 = S_1 = 1$: clear register to 0.

3. Construct a 16-bit serial-parallel counter, using four 4-bit parallel counters. Suppose that all added logic is AND gates and that serial connections are employed between the four counters. What is the maximum number of AND gates in a chain that a signal must propagate through in the 16-bit counter?

4. Using two binary counters of the type shown in Figure 7-14 of your textbook, and logic gates, construct a binary counter that counts from decimal 11 through decimal 233. Also, add an additional input and logic to the counter to initialize it synchronously to 11 when the signal INIT is 1.

5. Design a 4-bit BCD counter: (a) draw the state diagram and state table, (b) implement the counter using D flip-flops, T-flip-flops, SR flip-flops, and JK flip-flops.

6. The 4-bit Johnson counter advances through the sequence 0000, 1000, 1100, 1110, 1111, 0111, 0011, 0001, and then repeats. Using the standard counter design process show how to implement this counter using (a) D flip-flops and (b) T flip-flops.

7. Design a counter with the following repeated sequence: 0, 2, 1, 3, 4, 6, 5, 7, using D flip-flops.