ECE 213 -- Computer Organization and Microprocessors Laboratory

Course website: http://www.ece.ucy.ac.cy/courses/ECE213/

Spring 2010

COURSE SYLLABUS

Meeting Time: Monday OR Thursday, 8:00-10:00am, OR Tuesday, 3:30-5:30pm
Latsia, LA 130 laboratory

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Course Objectives

To provide an in-depth understanding of the underlying organization of modern computer systems and microprocessors via hands-on experience in design and implementation of such systems. The laboratory experiments include symbolic programming and simple microprocessor design using CAD tools and implementation using programmable devices.

Course Outcomes

- Practical understanding of computer organization and design.
- Practical experience in symbolic programming using MIPS Assembly and the SPIM simulator.
- Practical experience in microprocessor design and implementation using Computer-Aided Design tools, hardware description languages (such as VHDL), and programmable devices.
- Experience in design team work by participating in a large design project.

Prerequisites

ECE 212 (co-registration allowed) or demonstrated knowledge in all of the following:

- Computer programming
- Number systems
- Boolean Algebra
- Combinational and Sequential circuits
- Computer Organization and Microprocessors

Required Reading Material

- No required text.
- Laboratory notes and handouts.

Recommended Readings (with order of preference)

- D. A. Patterson and J. L. Hennessy, *Computer Organization and Design: The Hardware/Software Interface*, Morgan Kaufman, 3rd Ed., 2005.
- P. J. Ashenden, *The Student's Guide to VHDL, 2ed*, Morgan Kaufmann Publishers, 1998.
- D. Steetman, *See MIPS Run*, Morgan Kaufman, 2002.
- S Yalamanchili, *VHDL Starters Guide*, Prentice-Hall, 1998.
- E. Farquhar and P. Bunce, *The MIPS Programmer's Handbook,* Morgan Kaufman.
- M. M. Mano and C. R. Kime, *Logic and Computer Design Fundamentals,* Prentice-Hall, 3rd Ed., 2004.
- J. L. Hennessy and D. A. Patterson, *Computer Architecture: A Quantitative Approach,* Morgan Kauufman, 3rd Ed., 2003

Computer Usage

Programming in MIPS Assembly language and simulation using SPIM on a Linux platform. Also, use of Altera Quartus II for schematic and/or VHDL design and simulation.

Contents

The laboratory consists of two major parts:

- The first part involves symbolic programming in MIPS Assembly and use of the SPIM simulator extensively (on a Linux platform). Weekly assignments focus on practicing in different individual organizational issues, such as arithmetic function implementation, instruction addressing modes, program stack, decision and branching, program recursion, etc. System-level issues such as interrupts and I/O functions are considered in the project. Work is on an individual basis.
- The second part concentrates on design problems using the Altera Quartus II tools for schematic and/or VHDL design and simulation (Windows platform). A simple microprocessor is designed on a step-by-step basis and implemented using CPLD/FPGA based system boards. The different components of the microprocessor designed via weekly assignments, as well as the integration, verification and implementation are a group effort.

Work Expected from Students

- Required laboratory attendance.
- Regular readings of the assigned material.
- Weekly laboratory exercises and reports (typed).
- In-class laboratory exercises. Preparation PRIOR to laboratory is often required.
- Two laboratory projects and corresponding oral examinations.

Grading

MIPS Assembly – SPIM Exercises	15% (+5% for bonus exercise)
Project in MIPS Assembly	35%
Design Exercises	15%
Group Design Project	35%

Passing this course requires a total grade of at least 50% as well as satisfactory completion of BOTH laboratory projects. (Satisfactory completion means a grade of no less than 50%. The average grade in both projects will also be taken into account.)

The instructor reserves the right to make minor changes in the above grade distribution. Moreover, the instructor reserves the right to adjust borderline grades up or down based on attendance and class participation.

Course Policies

• **Grading:** Inquiries and disputes about graded work should be made **within one week** after it has been handed back. Only written inquiries that clearly explain the complaint will be considered. Not readable/sloppy work will incur an automatic 20% penalty, if accepted.

• **Late Work:** All work must **always** be turned in at the **beginning** of the class period of the day it is due. Late submissions incur a 20% penalty for each day being late, up to a maximum of 3 days after which no points will be granted. All extensions should be arranged with the instructor prior to the due date.

• **Absences:** Excused absences due to illness or approved University travel must follow University policy (singed note from health care provider, etc). No make-up laboratory exams or assignment due date extensions will be granted, unless your absence is excused. In the case of foreseen absences (such as approved University travel), you must contact your instructor prior to the related absence date.

• **Academic Honesty:** You are encouraged to work and talk with other students about laboratory exercises, assigned homework, and projects. **However, when writing your program code and documentation, the work must be solely your own.** Work that has significant overlap with another one is a violation of Academic Honesty and will imply zero points for all involved and will be reported to the Department Council. The instructor may use appropriate software to check the integrity of an exercise or a report.

• **Communication:** The instructor will maintain a list of student email addresses for timely dissemination of information regarding the class whenever necessary.