Overview

The rapid and on-going increase of the complexity of digital integrated circuits (ICs) requires the use of computer-aided design tools in order to effectively and efficiently design such large electronic systems. This course introduces the techniques of modelling digital systems at various abstraction levels, and the computer-aided design (CAD) algorithms that are applied to these models to support the various design and analysis tasks. This is not a “how-to” course on using CAD tools. Rather, it concentrates on the study of the algorithms used by CAD tools and the design methodologies they promote. The course will cover: modelling of digital systems for simulation and automated synthesis using modern hardware description languages (VHDL), logic synthesis and optimization, physical design automation (placement, floor-planning and routing) considering the CMOS technology, testing (fault models, simulation, basic test generation), timing analysis and verification.

Course Objective

To provide an introduction to the fundamentals of Computer-Aided Design tools for the modelling, design, analysis, test, and verification of digital Very Large Scale Integration (VLSI) systems.

Course Outcomes

- Establish comprehensive understanding of the various phases of CAD for digital electronic systems, from digital logic simulation to physical design, including test and verification.
- Demonstrate knowledge and understanding of fundamental concepts in CAD.
- Demonstrate knowledge of computational and optimization algorithms and tools applicable to solving CAD related problems.
- Establish capability for CAD tool development and enhancement.
Prerequisites
- Digital logic design (ECE210, ECE211)
- Data structures (CS034/035)
- C or C++ programming language

Topics
- Introduction to Application Specific Integrated Circuits (ASICs) and Electronic Design Automation
- Basic CMOS technology and design rules
- Overview of hardware modeling with VHDL
- Graph concepts, algorithms and their efficiency
- Simulation
- High-level synthesis: datapath and control synthesis
- Logic-level synthesis and optimization of combinational and sequential circuits
- Testing (fault modeling, simulation, test generation) and design for testability
- Physical design automation (placement, floorplanning, routing)
- Timing analysis
- Verification

Note: This is a long list to be studied in-depth! We will concentrate on fundamental concepts in each topic, and selected topics will be studied in more detail.

Reading Material & References
- Textbook: M.J.S. Smith, Application-Specific Integrated Circuits, Addison-Wesley Pub Co, 1997 (selected topics)
  http://www-ee.eng.hawaii.edu/~msmith/ASICs/HTML/ASICs.htm#anchor935203
- Class handouts, notes and research papers
  (selected topics from the following books will be used)

Computer Usage
Hardware modeling and simulation using the VHDL hardware description language. Laboratory exercises make use of popular commercial (Cadence) and academic CAD tools. Also, the course includes tool development using C/C++.

The major focus will be on tool development, not their usage!
Grading

Midterm Examination  30%
Final Examination     30%
Programming Project  20%
Laboratory Exercises (5-6) 15%
Homework Exercises (3-4)  5%

Passing the course requires:
• A total grade of at least 50%.
• Completion of project and all laboratory exercises.

The instructor reserves the right to make minor changes in the above grade distribution. Moreover, the instructor reserves the right to adjust borderline grades up or down based on attendance and class participation.

Course Policies

• **Grading**: Inquiries and disputes about graded work should be made **within one week** after it has been handed back. Not readable/sloppy work will incur an automatic 20% penalty, if accepted. Also, in order to get full credit you must show all of your computations.

• **Late Work**: All work must **always** be turned in at the **beginning** of the class period of the day it is due. Late submissions incur a 20% penalty for each day being late, up to a maximum of 3 days after which no points will be granted. All extensions should be arranged with the instructor prior to the due date.

• **Absences**: No make-up exams or homework assignment due date extensions will be granted, unless your absence is excused. In the case of foreseen absences (such as approved University travel), you must contact your instructor prior the related absence date.

• **Academic Honesty**: You are encouraged to work and talk with other students about lectures, homework/laboratory assignments, and exams preparation. **However, when writing your homework solutions, program code and documentation, the work must be solely your own.** Work that has significant overlap with another one is a violation of Academic Honesty and will be reported to the Department Council. The instructor may use appropriate software to check the integrity of a report.