

Call for Papers

IEEE Design & Test Special Issue on
Advances in 3D Integrated Circuits, Systems, and CAD Tools
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Guest Editors:

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Three-dimensional (3D) integration has become one of the most promising breakthrough technologies that can achieve higher integration density, better performance, and lower power. To enable 3D integration, academia and industry have researched various subjects such as manufacturing technologies, design and testing methodologies, optimization algorithms, heat dissipation, and reliability of inter-layer vias. Killer applications fully exploiting the benefits 3D integration provides such as core-memory stacking have also been actively researched. Thanks to the enormous research efforts put on 3D integration, a few prototype circuits have been fabricated in academia and industry and commercial products such as wide-I/O memory are finally about to be on the market in the near future.

Now, 3D integration is facing new problems and issues. For example, monolithic 3D integration is one of the most fine-grained 3D integration technologies proposed until now and enables much higher integration density than any other 3D integration technologies such as interposer- and through-silicon-via (TSV)-based integration. Because of the higher integration density without improved heat dissipation capabilities, however, monolithic 3D ICs have very serious routing congestion, power delivery, and thermal problems. Another problem 3D integration is facing is that 3D integration is still far behind the process scaling. 14nm chips are being fabricated and tested, and 10nm and even sub-10nm technology nodes are expected to be ready for mass production in the next few years. However, the performance and/or power benefits 3D integration provides are not satisfactory for adoption of 3D ICs in the high-performance and/or low-power chip markets. Rather, adopting the next-generation process technology might be more beneficial than adopting 3D integration technology. Therefore, the applicability of 3D integration technology is very limited as of now and the need for more innovative ideas on the application of 3D integration and more breakthrough design methodologies and optimization algorithms is ever increasing.

IEEE Design and Test seeks original manuscripts for a special issue on “Advances in 3D Integrated Circuits, Systems, and CAD Tools” scheduled for publication in July/August 2015. The topics of interest include, but are not limited to:

- Advances in the 3D integration technologies (monolithic, high-density TSVs, 2.5-D integration, cost-effective integration technologies, etc.)
- Advances in effective heat dissipation/mitigation for 3D integration (from technology- and hardware-level to architecture- and software-level)
- Advances in 3D network-on-chip (NoC), many-core/many-tier 3D NoC processors, innovative 3D NoC architectures
- New applications of 3D integration (high-bandwidth I/O for FPGA, wireless inter-chip communication, heterogeneous integration, applications in MEMS and sensors, etc.)
- 3D memory (Wide-I/O and high-bandwidth memory (HBM), hybrid memory cube (HMC), etc.)
- Advances in testing, thermal/reliability modeling, chip-package interaction analysis, cost analysis and modeling, yield improvement for 3D integrated circuits and

systems

- New, innovative design methodologies and optimization algorithms for 3D integrated circuits and systems
- The present and the future of CAD tools for 3D integration

Submission and review procedures

Prospective authors should follow the submission guidelines for IEEE Design & Test. All manuscripts must be submitted electronically to the IEEE Manuscript Central Web site at <http://www.manuscriptcentral.com/>. Indicate that you are submitting your article to the special issue on "Advances in 3D Integrated Circuits, Systems, and CAD Tools". All papers will undergo the standard IEEE Design & Test review process.

Schedule

- Submission deadline: December 1, 2014
- First round of reviews completed: February 15, 2015
- Revised manuscript due: March 15, 2015
- Notification of final acceptance: April 15, 2015
- Submission of final version: May 1, 2015
- Publication date: July/August 2015

Questions

Please direct questions regarding the special issue to guest editors Dae Hyun Kim (gtdae Hyun@gmail.com) and Sung Kyu Lim (limsk@ece.gatech.edu).