

Call for Papers
IEEE Design & Test Special Issue on
Silicon Nanophotonics for Future Multicore Architectures
Publication Date: September/October 2014

Guest Editors:

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The need for high performance and energy-efficient communication between processing cores has never been more critical. Rapidly increasing application complexity and limited computing power budgets have led to more and more lightweight cores replacing fewer bulky cores in emerging processor chips. The increase in core counts has put more pressure on the communication fabric which must now support many more streams of higher bandwidth data transfers than ever before. A direct consequence of this trend is that chip power and performance are now dominated not by processor cores but by the need to transport data between processors and to memory. Unfortunately, traditional electrical wires that make up the backbone of communication fabrics on computing chips today are facing unprecedented challenges in ultra-deep nanoscale CMOS fabrication technologies. These wires are becoming slower, more power hungry, and less reliable. We are thus at a critical juncture where the power, bandwidth, and latency of communication must scale favorably to meet the needs of processing chips in the near future. Silicon nanophotonics represents one of the more promising solutions to overcome the challenge of worsening communication performance with electrical wires. Such a solution also promises to pair well with existing board-to-board and chip-to-chip photonics offerings that are rapidly being adopted today.

IEEE Design and Test seeks original manuscripts for a special issue on “Silicon Nanophotonics for Future Multicore Architectures” scheduled for publication in Sep/Oct 2014. The topics of interest include, but are not limited to:

- Emerging silicon nanophotonic devices, technological innovations, and challenges
- Novel architectures that integrate silicon nanophotonics with computational resources, cache, DRAM, and wiring at the intra-chip level, for 2D and 3D chips.
- CAD tools for the design and analysis of silicon nanophotonic based systems
- Runtime techniques to adapt silicon nanophotonic components and related chip resources to multiple applications and workload perturbations.
- Mechanisms to model, quantify, and cope with thermal variations, process uncertainty, and failure for silicon nanophotonic components
- Impact of silicon nanophotonics on the spectrum of parallel applications from the embedded to the HPC domain.

Submission and review procedures

Prospective authors should follow the submission guidelines for IEEE Design & Test. All manuscripts must be submitted electronically to the IEEE Manuscript Central Web site at <http://www.manuscriptcentral.com/dandt>. Indicate that you are submitting your article to the special issue on “Silicon Nanophotonics for Future Multicore Architectures.” All papers will undergo the standard IEEE Design & Test review process. Submitted manuscripts must not have been previously published or currently submitted for publication elsewhere. Manuscripts must not exceed 5,000 words, including figures (with each average-size figure counting as 200 words) and a maximum of 12 references (50 for surveys). This amounts to about 4,000 words of text and a maximum of five small to medium figures.

Schedule

- Submission Deadline: 21st December 2013
- Reviews Complete: 1st March 2014
- Revisions Due: 15th April 2014
- Notification of final acceptance: 1st June 2014
- Submission of final version: 1st July 2014
- Publication date: September/October 2014