IEEE Design & Test

Special Issue Proposal

Special Issue on Future Landscape of Embedded Memories

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1. Context and Motivation for the Special Issue

Power dissipation has become the chief performance limiter in modern microprocessors – triggering a flurry of research activities on low power design techniques. One of the most effective ways to curb chip power is to integrate more memory: a larger cache memory improves micro-architectural performance with only a modest increase in CV^2f power. As a result, the past decade has seen a precipitous increase in the amount of on-die embedded memory. Approximately half the chip area is devoted to cache memory in state-of-the-art designs. For example, Intel's 8-core Nehalem processor has 24MB of shared L3 cache based on SRAM cells while IBM's POWER7 processor has a 32MB L3 cache built in an embedded DRAM (eDRAM) technology. The need for robust high-density embedded memories is projected to grow as designers continue to seek power-conscious ways to improve chip performance. The unique challenges and opportunities associated with embedded memory design make it a deserving topic for a special issue in the IEEE D&T magazine.

From the viewpoint of the circuit designer, embedded memory presents unique challenges as compared with logic circuits. In particular, memory bit cell functionality is often inherently susceptible to various noise margin issues. For example, the read and write operations of 6-transistor SRAM cells are "ratioed" by nature, which diminishes voltage margins at low supply voltages. Likewise, 1-transistor 1-capacitor eDRAM cells rely on the charge sharing to perform a read operation, which results in exposure to noise coupling, sense amplifier offsets, and other signal margin related problems. Memory density needs drive the use of minimum sized devices, which have significantly higher local mismatch, and tend to exacerbate these noise margin problems. To combat these issues, a tight coupling between the process development and

memory circuit/architecture design is indispensible. Device parameters are constantly tweaked to improve SRAM yield while the circuit design is optimized based on these new process parameters. Similarly, eDRAM circuit performance depends heavily on the characteristics of the specialized trench capacitors and access transistors. Emerging memory devices such as magnetic RAM (MRAM) and phase change RAM (PRAM), which have made great strides in recent years to become strong contenders against incumbent memories, present new tradeoffs that further emphasize the need for a holistic, cross-disciplinary evaluation.

In this proposed special issue, we will cover recent trends of various types of embedded memory and evaluate their future prospects. For mainstream memory, we will solicit papers on low voltage SRAM, eDRAM, embedded flash, and one-time-programmable ROM. In the emerging memory area, we will highlight the recent progress of novel future memory technologies such as MRAM, PRAM, FeRAM, floating body SOI RAM, thyrister RAM, and RRAM. The main focus will be on circuit design and its related areas such as test, architecture, modeling, system, and computer-aided-design. Contributions to this special issue will be encouraged from both industry and academia to provide a practical and forward-looking view of the future embedded memory landscape. To the best of our knowledge, the proposed theme does not overlap with any recently published special issue or those that are currently in preparation or in press.

2. Proposed Outline

A. A tutorial paper by an industry veteran on various types of embedded memory covering

- History, evolution and scaling trend of incumbent embedded memory technologies
- Key process and circuit innovations that have enabled unprecedented memory density
- Discussion on architecture, test and CAD level techniques for facilitating embedded memory development
- A progress update and comparison of different emerging memories
- On-going technical challenges and future outlook

B. Four to five articles covering different class of embedded memory:

- Two or three papers on mainstream embedded memory such as SRAM, eDRAM, embedded flash and one time programmable ROM.

- Two or three papers on emerging memory such as MRAM, PRAM, FeRAM, floating body SOI RAM, thyrister RAM, memrister based RAM, etc.
- Paper submissions will be encouraged from both industry and academia.
- Topics of interest are circuit design and its related areas such as test, architecture, modeling, system, and computer-aided-design

3. Sources of Contributions

We plan to attract submissions for the proposed special issue through a combination of the open call-for-papers and targeted solicitations. All submissions will be subject to the regular Design and Test review process. The call-for-papers will be advertised through various IEEE society mailing lists and distributed at relevant conferences.

Besides the open call-for-papers, we also plan targeted solicitations for contributions on each of the 5 topics suggested under Section 2.B. Some active researchers and experts in these areas are listed below:

Tutorial paper on embedded memory

1. <Names deleted>
2. <Names deleted>

SRAM

1. <Names deleted>
2. <Names deleted>

Embedded DRAM

1. <Names deleted>
2. <Names deleted>

Non volatile memory (one time programmable ROM, embedded flash)

1. <Names deleted>

Emerging memory (MRAM, PRAM, FeRAM, floating body SOI RAM, thyrister RAM, memrister RAM, etc)

1. <Names deeted>

4. Review Process

Each paper will be sent to 4 or 5 external reviewers. At least 3 reviews will be necessary to make a decision. The schedule will allow 4 weeks for paper review. The papers will be ranked by their relative score, and will receive an additional round of review by the guest editors to determine the final set of 5 accepted papers.

5. Proposed Schedule

- **Articles due for review: 15th May, 2010**
- **Reviews completed: 1st July, 2010**
- **Article revisions due: 15th August, 2010**
- **Notice of final acceptance: 1st September 2010**
- **All materials due to edit: 15th October 2010**
- **Publication date: January/February 2011**

Call for Papers

Special Issue on Future Landscape of Embedded Memories

Guest Editors: Chris H. Kim (University of Minnesota), Leland Chang (IBM TJ Watson Research Center)

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Embedded memory presents unique design challenges as compared with logic circuits. In particular, memory bit cell functionality is often inherently susceptible to various noise margin issues. Memory density needs drive the use of minimum sized devices, which have significantly higher local mismatch, and tend to exacerbate these noise margin problems. To combat these issues, a tight coupling between the process development and memory circuit/architecture design is indispensible. Emerging memory devices such as magnetic RAM (MRAM) and phase change RAM (PRAM), which have made great strides in recent years to become strong contenders against incumbent memories, present new tradeoffs that further emphasize the need for a holistic, cross-disciplinary evaluation.

IEEE Design and Test seeks original manuscripts for a special issue on "Future Landscape of Embedded Memory", scheduled for publication in January/February 2011. This special issue will cover recent design techniques for various low voltage embedded memories and evaluate their future prospects. Paper submissions are encouraged for both mainstream memory circuits (e.g. SRAM, eDRAM, embedded flash) as well as emerging memory technologies (e.g. MRAM, PRAM, FeRAM).

Topics of interest include (but are not limited to)

- High performance and low power SRAM
- Embedded DRAM (1T1C and gain-cell)

- Nonvolatile memory such as embedded flash and one-time-programmable memory
- Emerging memory such as MRAM, PRAM, FeRAM, floating body SOI RAM, thyrister RAM, and memrister RAM.
- Memory circuit techniques for mitigating noise issues and improving cell density
- Test, architecture, modeling, and computer-aided-design for embedded memory

Submission and review procedures

Prospective authors should follow the submission guidelines for *IEEE Design & Test.* All manuscripts must be submitted electronically to the IEEE Manuscript Central Web site at https://mc.manuscriptcentral.com/cs-ieee. Indicate that you are submitting your article to the special issue on ''Future Landscape of Embedded Memories''. All articles will undergo the standard *IEEE Design & Test* review process. Submitted manuscripts must not have been previously published or currently submitted for publication elsewhere. Manuscripts must not exceed 5,000 words, including figures (with each average-size figure counting as 200 words) and a maximum of 12 References (50 for surveys). This amounts to about 4,000 words of text and a maximum of five small to medium figures. Accepted articles will be edited for clarity, structure, conciseness, grammar, passive to active voice, logical organization, readability, and adherence to style. Please see IEEE D&T Author Resources at http://www.computer.org/dt/author.htm, then scroll down and click on Author Center for submission guidelines and requirements.

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Questions?

Please direct questions regarding this special issue to Guest Editors Chris H. Kim (chriskim@umn.edu) and Leland Chang (lelandc@us.ibm.com).