

ISVLSI 2019 Program Outline			
14 July (Sunday)	5:00 PM - 6:00 PM	Onsite Registration	
	6:00 PM - 8:00 PM	Welcome Reception/Cocktail WUF Panther Square	
15 July 2019 (Monday)	8:00 AM - 8:30 AM	Registration & Refreshment (Ballroom Foyer)	
	8:30 AM - 9:00 AM	Opening Remarks (Ballroom B)	
	9:00 AM - 9:45 AM	Keynote # 1 (Ballroom B)	
	9:45 AM - 10:00 AM	Coffee Break	Coffee Break
	10:00 AM - 11:00 AM	Session 1: Digital Circuits and FPGA based Designs I	Session 02: Special Session: FPGA Accelerator Design and Optimization
	11:00 AM - 12:00 PM	Session 3: System Design and Security I	Session 04: Special Session: FPGA Accelerator Design and Optimization
	12:00 PM - 1:15 PM	Lunch and Keynote (Ballroom B)	
	1:15 PM - 2:35 PM	Session 05: Computer-Aided Design and Verification I	Session 06: Special Session: NVM based Architecture and System
	2:35 PM - 2:50 PM	Coffee Break	Coffee Break
	2:50 PM - 4:10 PM	Session 07: Computer-Aided Design and Verification II	Session 08: Circuit, Reliability and Fault Tolerance I
	4:10 PM - 5:30 PM	Session 9: VLSI for Applied and Future Computing Technology I	Session 10: Special Session: Neuromorphic Computing and Emerging Technologies
	5:30 PM - 6:00 PM	ISVLSI Committee Meeting (WUC 245C)	
5:40 PM - 6:40 PM	Poster / Demo Session & Appetizers (Ballroom A)		
16 July 2019 (Tuesday)	8:30 AM - 9:00 AM	Refreshment (Ballroom B)	
	9:00 AM - 9:45 AM	Keynote # 2 (Ballroom B)	
	9:45 AM - 10:00 AM	Coffee Break	IEEE-CS TCVLSI Meeting (WUC 245C)
	10:00 AM - 11:00 AM	Session 11: Digital Circuits and FPGA based Designs II	Session 12: Special Session: Explorations in Energy-Efficient Computing for IoT Applications I
	11:00 AM - 12:00 PM	Session 13: Emerging and Post-CMOS Technologies I	Session 14: Special Session: Explorations in Energy-Efficient Computing for IoT Applications II
	12:00 PM - 1:00 PM	Lunch and Keynote (Ballroom B)	
	1:00 PM - 2:00 PM	Session 15: VLSI for Applied and Future Computing Technology II	Session 16: System Design and Security II
	2:00 PM - 3:20 PM	Session 17: Circuit, Reliability and Fault Tolerance II	Session 18: Special Session: Emerging Technologies and Architectures
	3:20 PM - 3:40 PM	Coffee Break	Coffee Break
	3:40 PM - 4:40 PM	Panel Discussion (Ballroom B)	
4:40 PM - 11:00 PM	Dinner Cruise and Award Ceremony		
17 July 2019 (Wednesday)	8:30 AM - 9:00 AM	Refreshment (Ballroom B)	
	9:00 AM - 9:45 AM	Keynote # 3 (Ballroom B)	
	9:45 AM - 10:00 AM	Coffee Break	Coffee Break
	10:00 AM - 11:00 AM	Session 19: System Design and Security III	Session 20: Special Session: Energy-Efficient Machine Learning
	11:00 AM - 12:20 PM	Session 21: Digital Circuits and FPGA based Designs III	Session 22: Special Session: Botnet of Things: Hardware Insecurity in the IoT Era
	12:20 PM - 1:00 PM	Lunch	
	1:00 PM - 2:00 PM	Session 23: Digital Circuits and FPGA based Designs IV	Session 24: Special Session: Secure, Smart, Connected Devices for Emergent Applications
	2:00 PM - 3:00 PM	Session 25: Emerging and Post-CMOS Technologies II	Session 26: System Design and Security IV
3:00 PM - 3:30 PM	Closing Remarks (Ballroom B)		

## KEYNOTE 1

9:00am ~ 9:45am, Monday July 15, 2019

*Ballroom B*

# Systems – An NSF Perspective



**Samee U. Khan**

**National Science Foundation and North Dakota State University**

### **Summary**

We are part of interesting times in which systems (compute, network, and storage) are rapidly evolving. These systems are the enablers for concepts of Smart Cities, Understanding the Human Brain, Humanoid Robots, Human Health, Fully Automated Data-driven Decision Systems, etc. This talk will describe NSF activities related to advancing systems and will include some personal observations on challenges and opportunities for the research community.

### **About Samee U. Khan**

Samee U. Khan received a PhD in 2007 from the University of Texas, Arlington, TX, USA. Currently, he is the Lead Program Director (Cluster Lead) for the Computer Systems Research at the National Science Foundation. He also is a faculty at the North Dakota State University, Fargo, ND, USA. His research interests include optimization, robustness, and security of computer systems. His work has appeared in over 400 publications. He is on the editorial boards of leading journals, such as ACM Computing Surveys, IEEE Access, IEEE Communications Surveys and Tutorials, IET Wireless Sensor Systems, IET Cyber-Physical Systems, and IEEE IT Pro. He is an ACM Distinguished Speaker, an IEEE Distinguished Lecturer, a Fellow of the Institution of Engineering and Technology (IET, formerly IEE), and a Fellow of the British Computer Society (BCS).

## LUNCHEON KEYNOTE

12:00pm ~ 1:15pm, Monday July 15, 2019

*Ballroom B*

### Challenges and Approaches for Future Secure Execution Environment Design



**Yan Solihin**

**Charles N. Millican Chair Professor of Computer Science at University of Central Florida**

#### **Summary**

Trustworthy software execution is increasingly demanded in multiple situations, including the cloud computing environment where customers execute their software in cloud servers, and in edge computing where computing may be performed on the edge nodes. Customers require strong privacy and security guarantees from a secure trust base in hardware. Recognizing this, chipmakers recently introduced secure execution environment, such as Intel SGX and AMD SEV. A key component of secure execution environment is memory encryption and integrity verification. In this talk, I will give an overview of key milestones in memory encryption and integrity verification technologies. Then, I will discuss how these technologies are not adequate in providing secure execution environment in the future, for several reasons. First, the threat model is incomplete. The pervasiveness of side channel vulnerabilities and attacks in both cloud servers and edge nodes can bypass the protection provided. Second, these technologies are not compatible with new persistent (or non-volatile) memory technologies that are coming online. I will approaches for designing future secure execution environment given the new challenges.

#### **About Yan Solihin**

Yan Solihin is a Charles N. Millican Chair Professor of Computer Science and Director for Cybersecurity and Privacy Cluster at the University of Central Florida. Prior to joining UCF, he was a Program Director at the National Science Foundation, with responsibilities in managing the Computer Systems Research (CSR) cluster, Scalable Parallelism in the eXtreme (SPX), and Secure and Trustworthy Cyberspace (SaTC), among others. He was also Professor of Electrical and Computer Engineering at NCSU from 2002 to 2018. In 2017, he was elected as an IEEE Fellow, recognized "for contributions to shared cache hierarchies and secure processors."

He obtained his B.S. degree in computer science from Institut Teknologi Bandung in 1995, B.S. degree in Mathematics from Universitas Terbuka Indonesia in 1995, M.A.Sc degree in computer engineering from Nanyang Technological University in 1997, and M.S. and Ph.D. degrees in computer science from the University of Illinois at Urbana-Champaign in 1999 and 2002. He is a recipient of 2010 and 2005 IBM Faculty Partnership Award, 2004 NSF Faculty Early Career Award, and 1997 AT&T Leadership Award. He is listed in the ISCA and HPCA Hall of Fame. His research interests include computer architecture, memory hierarchy design, non-volatile memory architecture, programming models, and workload cloning. He has published more than 70 papers in computer architecture and performance modeling, and authored 40+ patents. He has released several software packages to the public: ACAPP - a cache performance model toolset, HeapServer - a secure heap management library, Scaltool - parallel program scalability pinpointer, and Fodex - a forensic document examination toolset. He has written two graduate-level textbooks, including Fundamentals of Parallel Multicore Architecture, CRC Press, 2015.

## KEYNOTE 2

9:00am ~ 9:45am, Tuesday July 16, 2019

*Ballroom B*

# Can you trust your machine learning system?



**Sandip Kundu**

**National Science Foundation and University of Massachusetts at Amherst**

### **Summary**

Extensive integration of machine learning (ML) into critical applications like finance or healthcare demands an investigation of security of ML systems against malicious attacks. The various stages of the machine learning process, from data collection to model deployment present multiple avenues of attack that can compromise the integrity of a system. In this talk, we examine the three fundamental pillars of information security, namely, confidentiality, integrity and availability, with the machine learning process and categorize the various attacks against the three pillars. Confidentiality of an ML system involves securing it against exposure of the model parameters via the observation of responses and also, securing the original training dataset. Ensuring integrity of machine learning systems is a difficult task, but is crucial to prevent exploitation by adversaries. We conclude the talk with a discussion of potential defenses and a brief examination of future concerns.

### **About Sandip Kundu**

Sandip Kundu is a Program Director at the National Science Foundation in the CNS division within the CISE directorate. He is serving in this position on leave from the University of Massachusetts at Amherst, where he is a professor in Electrical and Computer Engineering Department. Kundu began his career at IBM Research as a Research Staff Member; then worked at Intel Corporation as a Principal Engineer before joining UMass Amherst as a professor in 2005. He has published over 250 research papers in VLSI design and test, holds several key patents including ultra-drowsy sleep mode in processors, and has given more than a dozen tutorials at various conferences. He is a Fellow of the IEEE, Fellow of the Japan Society for Promotion of Science (JSPS), Senior International Scientist of the Chinese Academy of Sciences and was a Distinguished Visitor of the IEEE Computer Society. He has served as an Associate Editor of the IEEE Transactions on Computers, IEEE Transactions on Dependable and Secure Computing, IEEE Transactions on VLSI Systems and ACM Transactions on Design Automation of Electronic Systems. He has been Technical Program Chair/General Chair of multiple conferences including ICCD, ATS, ISVLSI, DFTS and VLSI Design Conference.

## LUNCHEON KEYNOTE

12:00pm ~ 1:00pm, Tuesday July 16, 2019

*Ballroom B*

# VLSI in the era of internet of things ... and sensors



**Shekhar Bhansali**

**Department of Electrical and Computer Engineering,  
Florida International University, USA**

### **Summary**

The expected 4th technical revolution will be driven with connected devices and sensors. Key to this transformation is the cost of sensors and devices. This talk presents an overview of one such system a wearable sensor. It then articulates the needs for low cost, low speed, low complexity, low power (V)LSI and then explores whether VLSI will be the driver or the bottleneck for the 4th industrial revolution.

### **About Shekhar Bhansali**

Dr. Shekhar Bhansali currently serves as the Alcatel-Lucent Professor and Chair of the Department of Electrical and Computer Engineering at Florida International University (FIU), Miami, FL. His current research is in the areas of bio-sensing and bioengineering, oceanographic sensing, materials science, micro/nanotechnology and alternative energy. He has 36 U.S. Patents, edited two (2) books and published over 300 research articles. His research has been supported by the National Science Foundation (NSF), National Institutes of Health (NIH), industry (SRI, Draper and JCG) and national laboratories. He is a Fellow of National Academy of Inventors and has received numerous awards including FIU's Top Scholar Award in 2014, William R. Jones Outstanding Mentor Award from the Florida Education Fund in 2009 and 2011, Mentor of the Year Award from Alfred P. Sloan Foundation in 2009 and 2003 NSF CAREER award.

Dr. Bhansali has conceptualized and led a number of interdisciplinary graduate student research and training programs, including NSF-IGERT, NSF Bridge to Doctorate and Alfred P. Sloan Doctoral Fellowship Programs to increase diversity, retention and graduation rates. Through these programs, he oversaw the education of over 200 graduate students with multiyear fellowships in colleges of Engineering, Arts and Sciences, and Medicine. Dr. Bhansali is on the editorial boards of ISSS Journal of Micro and Smart Systems.

Dr. Bhansali received his doctoral degree in Electrical Engineering from RMIT University in Melbourne, Australia; his master's degree in Aircraft Production Engineering from the Indian Institute of Technology, Madras in Chennai, India; and his bachelor's degree with Honors in Metallurgical Engineering from the Malaviya Regional Engineering College in Jaipur, India.

## KEYNOTE 3

9:00am ~ 9:45am, Wednesday July 17, 2019

*Ballroom B*

# Is Moore's law ending and would it matter if it did?



**Rob Aitken**  
Fellow, ARM Research

### **Summary**

The demise of Moore's law has been predicted for decades, but over the last few years the pessimists have been able to point to rapidly approaching physical limits, skyrocketing chip development costs, and delays in process availability to support their argument. At the same time, however, new technologies are emerging, especially in memory and various forms of 3D stacking, and new architectures are being proposed, especially for machine learning and related problems. Meanwhile, both trends are causing previous challenges such as security, safety, and reliability to move to the forefront as key design issues. We clearly live in exciting times, but where will all this lead? This talk examines the present and looks at ways the future is unfolding and how it might continue to evolve.

### **About Rob Aitken**

Rob Aitken is an ARM Fellow and technology lead for ARM Research. He is responsible for technology direction of ARM research, including identifying disruptive technologies, monitoring the global technology landscape, and coordinating research efforts within and outside of ARM. His role includes developing strategic relationships with universities, consortia, and other key participants in the global research community. His research interests include emerging technologies, memory design, design for variability, resilient computing, and statistical design. He has published over 80 technical papers on a wide range of topics including impacts of technology scaling, statistics of memory bit cell variability and the use of static current monitoring as a circuit testing and diagnostic mechanism. He holds 30 US patents. Dr. Aitken joined ARM as part of its acquisition of Artisan Components in 2004. Prior to Artisan, he worked at Agilent and HP. He has given keynote addresses, tutorials and short courses at conferences and universities worldwide. He holds a Ph.D. from McGill University in Canada. Dr. Aitken is an IEEE Fellow, and serves as General Chair for the 2019 Design Automation Conference.

## **PANEL DISCUSSION**

**3:40pm ~ 4:40pm, Tuesday July 16, 2019**

*Ballroom B*

# **Hardware Intellectual Property (IP) Protection Techniques: Myth or Reality**

### **Chair & Moderator**

Jeyavijayan Rajendran - Texas A&M University

Gang Qu - University of Maryland

### **Panelists**

Rob Aitken, ARM Research

Siddharth Garg, NYU Tandon School of Engineering

Sandip Kundu, National Science Foundation

Ankur Srivastava, University of Maryland

### **Summary**

The fabless business model has given rise to many security threats including piracy of intellectual property (IP), overproduction, counterfeiting, reverse engineering (RE), and hardware Trojans (HT), severely undermining the benefits of the fabless model. Of these problems, protecting the IP has gained a special interest from the industry and government agencies as one wants to hide their “crown jewels” of hardware design. To this end, academia has developed a slew of techniques, companies are offering tools and services, and government agencies run research programs.

This panel will discuss the following:

- (a) Is the IP protection problem a real or a myth?
- (b) What are the state-of-the-art techniques? Do they deliver what has been promised?
- (c) How much is the industry willing to pay?
- (d) What are the outstanding challenges?

## SESSION 01

Monday July 15, 2019

Conference Room 221

### Digital Circuits and FPGA based Designs I

Chair: **Fernando Gehm Moraes, Escola Politécnica - PUCRS**

- 10:00 AM **\*Fast-ABC: A Fast Architecture for Bottleneck-Like Based Convolutional Neural Networks**  
*Xiaoru Xie (Nanjing University), Fangxuan Sun (Nanjing University), Jun Lin (Nanjing University), and Zhongfeng Wang (Nanjing University)*
- 10:20 AM **On-chip Instruction Generation for Cross-Layer CNN Accelerator on FPGA**  
*Yiming Hu (Tsinghua University), Shuang Liang (Tsinghua University), Jincheng Yu (Tsinghua University), Yu Wang (Tsinghua University), and Huazhong Yang (Tsinghua University)*
- 10:40 AM **T-DLA: An Open-source Deep Learning Accelerator for Ternarized DNN Models on Embedded FPGA**  
*Yao Chen (Advanced Digital Sciences Center, Singapore), Kai Zhang (Advanced Digital Sciences Center, Singapore, Nankai University, Tianjin, China), Cheng Gong (Nankai University, Tianjin, China), Cong Hao (University of Illinois at Urbana-Champaign, IL, USA), Xiaofan Zhang (University of Illinois at Urbana-Champaign, IL, USA), Tao Li (Nankai University, Tianjin, China), and Deming Chen (University of Illinois at Urbana-Champaign, IL, USA)*

## SESSION 02

Monday July 15, 2019

Conference Room 223

### Special Session: FPGA Accelerator Design and Optimization I

Chair: **Mohamad Hammam Alsafrjalani, University of Miami and Shi Sha, Wilkes University**

- 10:00 AM **Optimization of Convolutional Neural Networks on Resource Constrained Devices**  
*Arish S (Nanyang Technological University), Sharad Sinha (Indian Institute of Technology (IIT) Goa), and Smitha K G (Nanyang Technological University)*
- 10:20 AM **When Neural Architecture Search Meets Hardware Implementation: from Hardware Awareness to Co-Design**  
*Xinyi Zhang (University of Pittsburgh), Weiwen Jiang (University of Notre Dame), Yiyu Shi (University of Notre Dame), and Jingtong Hu (University of Pittsburgh)*
- 10:40 AM **A Cost-Effective CNN Accelerator Design with Configurable PU on FPGA**  
*Chi Fung Brian Fong (Hong Kong University of Science and Technology), Jiandong Mu (Hong Kong University of Science and Technology), and Wei Zhang (Hong Kong University of Science and Technology)*



## SESSION 03

Monday July 15, 2019

Conference Room 221

### System Design and Security I

Chair: **Xiaolin Xu, University of Illinois at Chicago**

- 11:00 AM **\*Transient Effect Ring Oscillators Leak Too**  
*Ugo Mureddu (Univ Lyon, UJM-Saint-Etienne, CNRS, Laboratoire Hubert Curien UMR 5516), Brice Colombier (Univ Lyon, UJM-Saint-Etienne, CNRS, Laboratoire Hubert Curien UMR 5516), Nathalie Bochard (Univ Lyon, UJM-Saint-Etienne, CNRS, Laboratoire Hubert Curien UMR 5516), Lilian Bossuet (Univ Lyon, UJM-Saint-Etienne, CNRS, Laboratoire Hubert Curien UMR 5516), and Viktor Fischer (Univ Lyon, UJM-Saint-Etienne, CNRS, Laboratoire Hubert Curien UMR 5516)*
- 11:20 AM **Not All Feed-Forward MUX PUFs Generate Unique Signatures**  
*Alex Ayling (University of Illinois), Satya Venkata Sandeep Avvaru (University of Minnesota), and Keshab Parhi (University of Minnesota)*
- 11:40 AM **SPN-DPUF: Substitution-Permutation Network based Secure Circuit for Digital PUF**  
*Johan Marconot (Univ, Grenoble Alpes, CEA, LETI, DSYS,; Univ. Grenoble Alpes , Grenoble INP), David Hely (Univ. Grenoble Alpes , Grenoble INP), and Florian Pebay-Peyroula (Univ, Grenoble Alpes, CEA, LETI)*

## SESSION 04

Monday July 15, 2019

Conference Room 223

### Special Session: FPGA Accelerator Design and Optimization II

Chair: **Mohamad Hammam Alsafrjalani, University of Miami and Shi Sha, Wilkes University**

- 11:00 AM **Area Efficient Box Filter Acceleration by Parallelizing with Optimized Adder Tree**  
*Xinzhe Liu (ShanghaiTech University), Fupeng Chen (ShanghaiTech University), and Yajun Ha (ShanghaiTech University)*
- 11:20 AM **Towards Efficient Compact Network Training on Edge-Devices**  
*Feng Xiong (Tsinghua University), Fengbin Tu (Tsinghua University), Shouyi Yin (Tsinghua University), and Shaojun Wei (Tsinghua University)*
- 11:40 AM **Near-Memory and In-Storage FPGA Acceleration for Emerging Cognitive Computing Workloads**  
*Ashutosh Dhar (University of Illinois), Sitao Huang (University of Illinois), Jinjun Xiong (University of Illinois; BM Research), Damir Jamsek (IBM Systems), Bruno Mesnet (IBM Systems), Jian Huang (University of Illinois), Nam Sung Kim (University of Illinois; Samsung), Wen-mei Hwu (University of Illinois), and Deming Chen (University of Illinois)*

## SESSION 05

Monday July 15, 2019

Conference Room 221

### Computer-Aided Design and Verification I

Chair: **K.G. Smitha**, Nanyang Technological University and **Shivam Swami**, Micron Technology

- 1:15 PM **Formal Verification of Integer Dividers: Division by a Constant**  
*Atif Yasin (University of Massachusetts Amherst), Tiankai Su (University of Massachusetts Amherst), Sébastien Pillement (University of Nantes, France), and Maciej Ciesielski (University of Massachusetts Amherst)*
- 1:35 PM **PageCmp: Bandwidth Efficient Page Deduplication through In-memory Page Comparison**  
*Mehrnoosh Raoufi (University of Pittsburgh), Quan Deng (National University of Defense Technology), Youtao Zhang (University of Pittsburgh), and Jun Yang (University of Pittsburgh)*
- 1:55 PM **An ESL Environment for Modeling Electrical Interconnect Faults**  
*Nooshin Nosrati (University of Tehran), Katayoon Basharkhah (University of Tehran), Rezgar Sadeghi (University of Tehran), and Zainalabedin Navabi (University of Tehran)*
- 2:15 PM **Morphed Standard Cell Layouts for Pin Length Reduction**  
*Cheng-Wei Tai (Yuan Ze University) and Rung-Bin Lin (Yuan Ze University)*

## SESSION 06

Monday July 15, 2019

Conference Room 223

### Special Session: NVM based Architecture and System

Chair: **Yao Chen**, UIUC

- 1:15 PM **The Power of Orthogonality**  
*Sébastien Ollivier (University of Pittsburgh), Donald Kline Jr. (University of Pittsburgh), Roxy Kawsher (University of South Florida), Rami Melhem (University of Pittsburgh), Sanjukta Banja (University of South Florida), and Alex K. Jones (University of Pittsburgh)*
- 1:35 PM **In-memory AES Implementation for Emerging Non-volatile Main Memory**  
*Mimi Xie (University of Pittsburgh), Yawen Wu (University of Pittsburgh), Zhengge Jia (University of Pittsburgh), and Jingtong Hu (University of Pittsburgh)*
- 1:55 PM **Investigating Fairness in Disaggregated Non-Volatile Memories**  
*Vamsee Reddy Kommareddy (University of Central Florida), Clayton Hughes (Sandia National Laboratories), Simon Hammond (Sandia National Laboratories), and Amro Awad (University of Central Florida)*
- 2:15 PM **Pj-AxMTJ: Processing-in-memory with Joint Magnetization Switching for Approximate Computing in Magnetic Tunnel Junctions**  
*Hao Cai (Southeast University), Honglan Jiang (Institute of Microelectronics, Tsinghua University), Menglin Han (Southeast University), Zhaohao Wang (Beihang University), You Wang (Beihang University), Jun Yang (Southeast University), Jie Han (University of Alberta), Leibo Liu (Institute of Microelectronics, Tsinghua University), and Weisheng Zhao (Beihang University)*

## SESSION 07

Monday July 15, 2019

Conference Room 221

### Computer-Aided Design and Verification II

Chair: **Alex Jones, University of Pittsburgh**

- 2:50 PM **\*Dark-Silicon Inspired Energy Efficient Hierarchical TDM NoC**  
*Salma Hesham (Ruhr University Bochum, Germany, German University in Cairo, Egypt), Diana Goehringer (Technische Universitaet Dresden, Germany), and Mohamed A. Abd El Ghany (German University in Cairo, Egypt)*
- 3:10 PM **Traffic Driven Automated Synthesis of Network-on-Chip from Physically Aware Behavioral Specification**  
*Anup Gangwar (Arm, Inc.), Zheng Xu (Arm, Inc.), Nitin Kumar Agarwal (Arm, Inc.), Ravishankar Sreedharan (Arm, Inc.), and Ambica Prasad (Arm, Inc.)*
- 3:30 PM **Automated Communication and Floorplan-Aware Hardware/Software Co-Design for SoC**  
*Jong Bin Lim (University of Illinois at Urbana-Champaign) and Deming Chen (University of Illinois at Urbana-Champaign)*
- 3:50 PM **Computationally Efficient Learning of Quality Controlled Word Embeddings for Natural Language Processing**  
*Mohammed Alawad (Oak Ridge National Laboratory) and Georgia Tourassi (Oak Ridge National Laboratory)*

## SESSION 08

Conference Room 223

Monday July 15, 2019

### Circuit, Reliability and Fault Tolerance I

Chair: **Gert Jervan, Tallinn University of Technology**

- 2:50 PM **Formal Hardware Verification of InfoSec Primitives**  
*Mohamed Asan Basiri M (IIT KANPUR) and Sandeep K Shukla (IIT Kanpur)*
- 3:10 PM **SRAM On-chip Monitoring Methodology for Energy Efficient Memory Operation at Near Threshold Voltage**  
*Taehwan Kim (Seoul National University, Korea), Kwangok Jeong (Samsung Electronics Co., Ltd.), Taewhan Kim (Seoul National University, Korea), and Kyumyung Choi (Seoul National University, Korea)*
- 3:30 PM **Energy and Error Reduction using Variable Bit-width Optimization on Dynamic Fixed Point Format**  
*Mingze Gao (University of Maryland, College Park), Qian Wang (University of Maryland, College Park), and Gang Qu (University of Maryland, College Park)*
- 3:50 PM **Machine Learning-Based Processor Adaptability Targeting Energy, Performance, and Reliability**  
*Anderson Luiz Sartor (Carnegie Mellon University (CMU)), Pedro Henrique Exenberger Becker (Universidade Federal do Rio Grande do Sul (UFRGS)), Stephan Wong (Delft University of Technology (TU Delft)), Radu Marculescu (Carnegie Mellon University (CMU)), and Antonio Carlos Schneider Beck (Universidade Federal do Rio Grande do Sul)*

## SESSION 09

Monday July 15, 2019

Conference Room 221

### VLSI for Applied and Future Computing Technology I

Chair: **Nithin Kumar Y. B**, NIT Goa

- 4:10 PM **Energy-Efficient Embedded Inference of SVMs on FPGA**  
*Osman Elgawi (Sultan Qaboos University), A. M. Mutawa (Kuwait University), and Afaq Ahmad (Sultan Qaboos University)*
- 4:30 PM **A Reconfigurable Layered-Based Bio-Inspired Smart Image Sensor**  
*Pankaj Bhowmik (University of Florida), Md Jubaer Hossain Pantho (University of Florida), Sujan Saha (University of Florida), and Christophe Bobda (University of Florida)*
- 4:50 PM **An Asynchronous Analog to Digital Converter for Video Camera Applications**  
*Sunil R. (Vignan's Foundation for Science, Technology & Research, Guntur, A.P., India), Siddharth R.K. (National Institute of Technology Goa, India), Nithin Kumar Y.B. (National Institute of Technology Goa, India), and Vasantha M.H. (National Institute of Technology Goa, India)*
- 5:10 PM **Design of Switched-Current Based Low-Power PIM Vision System for IoT Applications**  
*Zheyu Liu (Tsinghua University), Zichen Fan (Tsinghua University), Qi Wei (Tsinghua University), Xing Wu (East China Normal University), Fei Qiao (Tsinghua University), Ping Jin (Tsinghua University), Xin-jun Liu (Tsinghua University), Chengliang Liu (Shanghai Jiao Tong University), and Huazhong Yang (Tsinghua University)*

## SESSION 10

Monday July 15, 2019

Conference Room 223

### Special Session: Neuromorphic Computing and Emerging Technologies

Chair: **Xueqing Li**, Tsinghua University

- 4:10 PM **IDE Development, Logic Synthesis and Buffer/Splitter Insertion Framework for Adiabatic Quantum-Flux-Parametron Superconducting Circuits**  
*Ruizhe Cai (Northeastern University), Xiaolong Ma (Northeastern University), Olivia Chen (Yokohama National University), Ao Ren (Northeastern University), Ning Liu (Northeastern University), Nobuyuki Yoshikawa (Yokohama National University), and Yanzhi Wang (Northeastern University)*
- 4:30 PM **A Framework for the Analysis of Throughput-Constraints of SNNs on Neuromorphic Hardware.**  
*Adarsha Balaji (Drexel University) and Anup Das (Drexel University)*
- 4:50 PM **Accelerating Deep Neural Networks in Processing-in-Memory Platforms: Analog or Digital Approach?**  
*Shaahin Angizi (University of Central Florida), Zhezhi He (University of Central Florida), Dayane Reis (University of Notre Dame), Xiaobo Sharon Hu (University of Notre Dame), Wilman Tsai (TSMC), Shy Jay Lin (TSMC), and Deliang Fan (University of Central Florida)*
- 5:10 PM **Exploiting Near-Memory Processing Architectures for Bayesian Neural Networks Acceleration**  
*Yinglin Zhao (Beihang University), Jianlei Yang (Beihang University), Xiaotao Jia (Beihang University), Xueyan Wang (Beihang University), Zhaohao Wang (Beihang University), Wang Kang (Beihang University), Youguang Zhang (Beihang University), and Weisheng Zhao (Beihang University)*

## POSTER SESSION

5:40pm ~ 6:40pm, Monday July 15, 2019

Ballroom B

Chair: **Gang Quan**, Florida International University

- P1 An Area Effective Programmable Front-end Amplifier for Neural Signal Acquisition**  
*Gopabandhu Hota (IIT Kharagpur), Hardik Agrawal (IIT Kharagpur), and Mrigank Sharad (IIT Kharagpur)*
- P2 Minimization of Flare in EUVL by Simultaneous Wire Segment Perturbation and Dummification**  
*Sudipta Paul (Indian Statistical Institute, Kolkata, India, University of Calcutta, Kolkata, India), Pritha Banerjee (University of Calcutta, Kolkata, India), and Susmita Sur-Kolay (Indian Statistical Institute, Kolkata, India)*
- P3 Exploration and Exploitation of Dual Timing Margins for Improving Power Efficiency of Variable-Latency Designs**  
*Ning-Chi Huang (National Chiao Tung University), Yu-Guang Chen (Yuan Ze University), and Kai-Chiang Wu (National Chiao Tung University)*
- P4 Improving Logic Optimization in Sequential circuits using Majority-inverter Graphs**  
*Walter Lau Neto (University of Utah), Xifan Tang (University of Utah), Max Austin (University of Utah), Luca Amaru (Synopsys Inc.), and Pierre-Emmanuel Gaillardon (University of Utah)*
- P5 Design of a CMOS Broadband Transimpedance Amplifier With Floating Active Inductor**  
*Xiangyu Chen (Gifu University) and Yasuhiro Takahashi (Gifu University)*
- P6 Distributed Pulse Rotary Traveling Wave VCO: Architecture and Design**  
*Prashansa Mukim (University of California Santa Barbara), Aditya Dalakoti (University of California Santa Barbara), David McCarthy (University of California Santa Barbara), Brandon Pon (University of California Santa Barbara), Carrie Segal (University of California Santa Barbara), Merritt Miller (University of California Santa Barbara), James F. Buckwalter (University of California Santa Barbara), and Forrest Brewer (University of California Santa Barbara)*
- P7 Test Your Test Programs Pre-Silicon: A Virtual Test Methodology for Industrial Design Flows**  
*Sebastian Pointner (Johannes Kepler University), Oliver Frank (Infineon Technologies Austria), Christoph Hazott (Infineon Technologies Austria), and Robert Wille (Johannes Kepler University)*
- P8 Design of a Safe Convolution Neural Network Accelerator**  
*Zheng Xu (University of Texas at Austin) and Jacob Abraham (University of Texas at Austin)*
- P9 Test Point Insertion Using Artificial Neural Networks**  
*Yang Sun (Auburn University) and Spencer Millican (Auburn University)*
- P10 Evaluation of Compilers Effects on OpenMP Soft Error Resiliency**  
*Jonas Gava (UFRGS), Vitor Bandiera (UFRGS), Ricardo Reis (UFRGS), and Luciano Ost (Loughborough University)*
- P11 A One-Cycle FIFO Buffer for Memory Management Software in Manycore Systems**  
*Ann Gordon-Ross (University of Florida), Saleh Abdel-Hafeez (Jordan University of Science and Technology), and Mohamad Hammam Alsafrjalni (University of Miami)*
- P12 Impact of Autocorrelation on Stochastic Circuit Accuracy**  
*Timothy Baker (University of Michigan) and John Hayes (University of Michigan)*
- P13 A Novel Single/Double Precision Normalized IEEE 754 Floating-Point Adder/Subtractor**  
*Brett Mathis (Oklahoma State University) and James Stine (Oklahoma State University)*
- P14 Tackling the Drawbacks of a Lagrangian Relaxation Based Discrete Gate Sizing Algorithm**  
*Henrique Placido (Universidade Federal do Rio Grande do Sul) and Ricardo Reis (Universidade Federal do Rio Grande do Sul)*

- P15 **A Dual-Band CMOS Low-Noise Amplifier using Memristor-Based Tunable Inductors**  
*Nicolas Wainstein (Technion - Israel Institute of Technology), Tamir Tsabari (Technion - Israel Institute of Technology), Yarden Goldin (Technion - Israel Institute of Technology), Eilam Yalon (Technion - Israel Institute of Technology), and Shahar Kvatinsky (Technion - Israel Institute of Technology)*
- P16 **Micro-electrode-dot array based Biochips : Advantages of Using Different Shaped CMAs**  
*Pampa Howladar (Indian Institute of Engineering Science and Technology, Shibpur), Pranab Roy (Indian Institute of Engineering Science and Technology, Shibpur), and Hafizur Rahaman (Indian Institute of Engineering Science and Technology, Shibpur)*
- P17 **An Improved Automatic Hardware Trojan Generation Platform**  
*Shichao Yu (Queen's University Belfast), Weiqiang Liu (Nanjing University of Aeronautics and Astronautics), and Maire O'Neill (Queen's University Belfast)*
- P18 **TrustFlow: A Trusted Memory Support for Data Flow Integrity**  
*Cyril Bresch (Univ. Grenoble Alpes, Grenoble INP, LCIS), David Hély (Univ. Grenoble Alpes, Grenoble INP, LCIS), Stéphanie Chollet (Univ. Grenoble Alpes, Grenoble INP, LCIS), and Ioannis Parissis (Univ. Grenoble Alpes, Grenoble INP, LCIS)*
- P19 **Enabling Microarchitectural Randomization in Serialized AES Implementations to Mitigate Side Channel Susceptibility**  
*Siva Nishok Dhanuskodi (University of Massachusetts, Amherst, USA) and Daniel Holcomb (University of Massachusetts, Amherst, USA)*
- P20 **Securing a Wireless Network-on-Chip against Jamming based Denial-of-Service Attacks**  
*Abhishek Vashist (Rochester Institute of Technology), Andrew Keats (Rochester Institute of Technology), Sai Manoj Pudukotai Dinakarrao (George Mason University), and Amlan Ganguly (Rochester Institute of Technology)*
- P21 **FAST: A Frequency-Aware Skewed Merkle Tree for FPGA-Secured Embedded Systems**  
*Yu Zou (University of Central Florida) and Mingjie Lin (University of Central Florida)*
- P22 **Defense-Net: Defend Against a Wide Range of Adversarial Attacks through Adversarial Detector**  
*Adnan Siraj Rakin (University of Central Florida) and Deliang Fan (University of Central Florida)*
- P23 **Deep State Encryption for Sequential Logic Circuits**  
*Yasaswy Kasarabada (University of Cincinnati), Sudheer Ram Thulasi Raman (University of Cincinnati), and Ranga Vemuri (University of Cincinnati)*

## RESEARCH DEMO SESSION

5:40pm ~ 6:40pm, Monday July 15, 2019

Ballroom B

Chair: **Himanshu Thapliyal, University of Kentucky**

- D1 fiction: Electronic Design Automation for Field-coupled Nanocomputing Circuits**  
*Marcel Walter (University of Bremen), Robert Wille (Johannes Kepler University Linz), Frank Sill Torres (DFKI GmbH), Daniel Grosse (University of Bremen & DFKI GmbH) and Rolf Drechsler (University of Bremen)*
- D2 Identifying the Origin of DRAM Manufacturer**  
*B. M. Bahar Talukder (University of Alabama in Huntsville) and M. Tauhidur Rahman (University of Alabama in Huntsville)*
- D3 Demonstration of Hardware Trojans in 3D ICs**  
*Zhiming Zhang (University of New Hampshire) and Qiaoyan Yu (University of New Hampshire)*
- D4 Research Demo of a Piezoelectric Based PUF for Hardware Security in IoT Devices**  
*Carson Labrado (University of Kentucky), Himanshu Thapliyal (University of Kentucky) and Zachary Kahleifeh (University of Kentucky)*

## STUDENT RESEARCH FORUM

5:40pm ~ 6:40pm, Monday July 15, 2019

Ballroom B

Chair: **Muhammad Shafique, Vienna University of Technology**

**Selcuk Kose, University of Rochester**

- F1 A Multi-Phases Time-to-Digital Converter With a Differential Vernier Ring oscillator**  
*annagrebah amina (Lyon Institute of Nuclear Physics), E. Bechetoille (Lyon Institute of Nuclear Physics), I.B. Laktineh (Lyon Institute of Nuclear Physics), H. Chanal (Lyon Institute of Nuclear Physics), P. Russo (Lyon Institute of Nuclear Physics), and H. Mathez (Lyon Institute of Nuclear Physics)*
- F2 ASSET: Architectures for Smart Security of Non-Volatile Memories**  
*Shivam Swami (University of Pittsburgh) and Kartik Mohanram (University of Pittsburgh)*
- F3 IRC: Cross-layer design exploration of Intermittent Robust Computation units for IoTs**  
*Arman Roohi (University of Central Florida) and Ronald F. DeMara (University of Central Florida)*
- F4 Design of Quantum Circuits for Cryptanalysis and Image Processing Applications**  
*Edgard Muñoz-Coreas (University of Kentucky) and Himanshu Thapliyal (University of Kentucky)*
- F5 Effect of Loop Positions on Reliability and Attack Resistance of Feed-Forward PUFs**  
*Satya Venkata Sandeep Avvaru (University of Minnesota) and Keshab Parhi (University of Minnesota)*
- F6 A Case Study On Approximate FPGA Design With an Open-Source Image Processing Platform**  
*Yunxiang Zhang (University of Houston Clear Lake), Xiaokun Yang (University of Houston Clear Lake), Lei Wu (Auburn University at Montgomery), and Jean Andrian (Florida International University)*
- F7 Real-Time Automatic Music Transcription (AMT) with Zync FPGA**  
*Kevin Vaca (University of Houston Clear Lake), Archit Gajjar (University of Houston Clear Lake), and Xiaokun Yang (University of Houston Clear Lake)*

## SESSION 11

Tuesday July 16, 2019

Conference Room 221

### Digital Circuit and FPGA Based Designs II

Chair: **Susmita Sur-Kolay**, Indian Statistical Institute

- 10:00 AM **An Approximate Multiply-Accumulate Unit with Low Power and Reduced Area**  
*Tongxin Yang (Logic Research Co., Ltd.), Toshinori Sato (Fukuoka University), and Tomoaki Ukezono (Tomoaki Ukezono)*
- 10:20 AM **A Low-Power Recurrence-Based Radix 4 Divider Using Signed-Digit Addition**  
*Matthew Gaalswyk (Oklahoma State University) and James Stine (Oklahoma State University)*
- 10:40 AM **Towards Data-Driven Approximate Circuit Design**  
*Ling Qiu (Clemson University), Ziji Zhang (University of Electronic Science and Technology of China), Jon Calhoun (Clemson University), and Yingjie Lao (Clemson University)*

## SESSION 12

Tuesday July 16, 2019

Conference Room 223

### Special Session: Explorations in Energy-Efficient Computing for IoT Applications I

Chair: **Yasuhiro Takahashi**, Gifu University and **Xunzhao Yin**, The University of Notre Dame

- 10:00 AM **MRAM-based Stochastic Oscillators for Adaptive Non-Uniform Sampling of Sparse Signals in IoT Applications**  
*Soheil Salehi (University of Central Florida), Alireza Zaeemzadeh (University of Central Florida), Adrian Tatulian (University of Central Florida), Nazanin Rahnavard (University of Central Florida), and Ronald F. DeMara (University of Central Florida)*
- 10:20 AM **Evaluation of Power Analysis Attacks on Cryptographic Circuit Using Adiabatic Logic**  
*Hiroki Koyasu (Gifu University) and Yasuhiro Takahashi (Gifu University)*
- 10:40 AM **Approximate Energy Recovery 4-2 Compressor for Low-Power Sub-GHz IoT Applications**  
*Himanshu Thapliyal (University of Kentucky) and Zachary Kahleifeh (University of Kentucky)*



## SESSION 13

Tuesday July 16, 2019

Conference Room 221

### Emerging and Post-CMOS Technologies I

Chair: **Na Gong**, University of South Alabama

- 11:00 AM **\*Routing Performance Optimization for Homogeneous droplets onMEDA based Digital Microfluidic Biochips**  
*Sarit Chakraborty (Government College of Engineering and Leather Technology, Kolkata, India) and Susanta Chakraborty (IEST, Shibpur)*
- 11:20 AM **Time-Constrained Sample Preparation Algorithm for Reactant Minimization on Digital Microfluidic Biochips**  
*Ling-Yen Song (National Chiao Tung University, Taiwan), Yu-Ying Li (National Chiao Tung University, Taiwan), Yung-Chun Lei (National Chiao Tung University, Taiwan), and Juinn-Dar Huang (National Chiao Tung University, Taiwan)*
- 11:40 AM **Logic Synthesis for Hybrid CMOS-ReRAM Sequential Circuits**  
*Saman Fröhlich (University of Bremen, Germany), Saeideh Shirinzadeh (University of Bremen, Germany), and Rolf Drechsler (University of Bremen, Germany)*

## SESSION 14

Tuesday July 16, 2019

Conference Room 223

### Special Session: Explorations in Energy-Efficient Computing for IoT Applications II

Chair: **Yasuhiro Takahashi**, Gifu University and **Xunzhao Yin**, The University of Notre Dame

- 11:00 AM **Ferroelectric FET based TCAM Designs for Energy Efficient Computing**  
*Xunzhao Yin (University of Notre Dame), Dayane Reis (University of Notre Dame), Michael Niemier (University of Notre Dame), and Xiaobo Sharon Hu (University of Notre Dame)*
- 11:20 AM **Post-Layout Simulation of Quasi-Adiabatic Logic Based Physical Unclonable Function**  
*Yasuhiro Takahashi (Gifu University), Hiroki Koyasu (Gifu University), S. Dinesh Kumar (University of Kentucky), and Himanshu Thapliyal (University of Kentucky)*
- 11:40 AM **A 1.8mW Perception Chip with Near-Sensor Processing Scheme for Low-Power AIoT Applications**  
*Zheyu Liu (Tsinghua University), Erxiang Ren (Beijing Jiaotong University), Li Luo (Beijing Jiaotong University), Qi Wei (Tsinghua University), Xing Wu (East China Normal University), Xueqing Li (Tsinghua University), Fei Qiao (Tsinghua University), Xin-Jun Liu (Tsinghua University), and Huazhong Yang (Tsinghua University)*

## SESSION 15

Tuesday July 16, 2019

Conference Room 221

### VLSI for Applied and Future Computing Technology II

Chair: **Yanzhi Wang, Northeastern University**

- 1:00 PM **\*Linear Optimization for Memristive Device in Neuromorphic Hardware**  
*Jingyan Fu (North Dakota State University), Zhiheng Liao (North Dakota State University), Na Gong (University of South Alabama), and Jinhui Wang (University of South Alabama)*
- 1:20 PM **Neuromorphic Image Sensor Design with Region-Aware Processing**  
*Md Jubaer Hossain Pantho (University of Florida), Pankaj Bhowmik (University of Florida), and Christophe Bobda (University of Florida)*
- 1:40 PM **CSrram: Area-Efficient Low-Power Ex-Situ Training Framework for Memristive Neuromorphic Circuits Based on Clustered Sparsity**  
*Arash Fayyazi (University of Southern California), Souvik Kundu (University of Southern California), Shahin Nazarian (University of Southern California), Peter A. Beerel (University of Southern California), and Massoud Pedram (University of Southern California)*

## SESSION 16

Tuesday July 16, 2019

Conference Room 223

### System Design and Security II

Chair: **Qiaoyan Yu, University of New Hampshire**

- 1:00 PM **Security in Many-Core SoCs Leveraged by Opaque Secure Zones**  
*Luciano Caimi (UFFS) and Fernando Gehm Moraes (PUCRS)*
- 1:20 PM **CAESAR-MPSoC: Dynamic and Efficient MPSoC Security Zones**  
*Siavoosh Payandeh Azad (Tallinn University of Technology), Gert Jervan (Tallinn University of Technology), Michael Tempelmeier (Technical University of Munich), and Johanna Sepúlveda (Technical University of Munich)*
- 1:40 PM **Modeling Hardware Trojans in 3D ICs**  
*Zhiming Zhang (University of New Hampshire) and Qiaoyan Yu (University of New Hampshire)*

## SESSION 17

Tuesday July 16, 2019

Conference Room 221

### Circuit, Reliability and Fault Tolerance II

Chair: Xiaokun Yang, University of Houston

- 2:00 PM **\*A Low-Complexity RS Decoder for Triple-Error-Correcting RS Codes**  
*Zengchao Yan (Nanjing University), Jun Lin (Nanjing University), and Zhongfeng Wang (Nanjing University)*
- 2:20 PM **Optimization of Comparator Selection Algorithm for TIQ Flash ADC Using Dynamic Programming Approach**  
*Ali Ozdemir (Pennsylvania State University), Mshabab Alrizah (Pennsylvania State University), and Kyusun Choi (Pennsylvania State University)*
- 2:40 PM **TSV-IaS: Analytic analysis and low-cost non-preemptive on-line detection and correction method for TSV defects**  
*Khanh Dang (Vietnam National University Hanoi), Akram Ben Ahmed (Keio University, Japan), Abderazek Ben Abdallah (The University of Aizu, Japan), and Xuan-Tu Tran (Vietnam National University Hanoi)*
- 3:00 PM **Energy-efficient Analog Processing Architecture for Direction of Arrival with Microphone Array**  
*Changlu Liu (Tsinghua University), Tianxiang Lan (Beijing Institute of Technology), Qin Li (Tsinghua University), Kaige Jia (Tsinghua University), Yidian Fan (Beihang University), Xing Wu (East China Normal University), Fei Qiao (Tsinghua University), Wei Qi (Tsinghua University), Xin-Jun Liu (Tsinghua University), and Huazhong Yang (Tsinghua University)*

## SESSION 18

Tuesday July 16, 2019

Conference Room 223

### Special Session: Emerging Technologies and Architectures

Chair: Surajeet Ghosh, Indian Institute of Engineering Science & Technology

- 2:00 PM **iMACE: In-Memory Acceleration of Classic McEliece Encoder**  
*Karthikeyan Nagarajan (Pennsylvania State University), Sina Sayyah Ensan (Pennsylvania State University), Swagata Mandal (Jalpaiguri Government Engineering College), Swaroop Ghosh (Pennsylvania State University), and Anupam Chattopadhyay (Nanyang Technological University)*
- 2:20 PM **Accelerating Compact Convolutional Neural Network with Multi-threaded Data Streaming**  
*Weiguang Chen (Shenzhen Institutes of Advanced Technology, Chinese Academy of Sciences, Shenzhen, China, University of Chinese Academy of Sciences, China), Zheng Wang (Shenzhen Institutes of Advanced Technology, Chinese Academy of Sciences, Shenzhen, China), Shanliao Li (Guilin University of Electronic Technology, Guilin, China), Zhibin Yu (Shenzhen Institutes of Advanced Technology, Chinese Academy of Sciences, Shenzhen, China), and Huijuan Li (Shenzhen Institutes of Advanced Technology, Chinese Academy of Sciences, Shenzhen, China)*
- 2:40 PM **Design of a Hierarchical Clos-Benes Optical Network-on-Chip Architecture**  
*Renjie Yao (Shanghai Jiao Tong University), Yaoyao Ye (Shanghai Jiao Tong University), and Weichen Liu (Nanyang Technological University, Singapore)*
- 3:00 PM **Machine Learning-based Prediction for Phase-based Dynamic Architectural Specialization**  
*Ruben Vazquez (University of Florida), Islam Badreldin (University of Florida), Mohamad Hammam Alsafrjalani (University of Miami), and Ann Gordon-Ross (University of Florida)*

## SESSION 19

Wednesday July 17, 2019

Conference Room 221

### System Design and Security III

Chair: **Ujjwal Guin, Auburn University**

- 10:00 AM **Hybrid Memristor-CMOS Obfuscation Against Untrusted Foundries**  
*Amin Rezaei (Northwestern University), Jie Gu (Northwestern University), and Hi Zhou (Northwestern University)*
- 10:20 AM **Memory Locking: An Automated Approach to Processor Design Obfuscation**  
*Michael Zuzak (University of Maryland, College Park) and Ankur Srivastava (University of Maryland, College Park)*
- 10:40 AM **Hardware-Software Co-Design Based Obfuscation of Hardware Accelerators**  
*Abhishek Chakraborty (University of Maryland College Park) and Ankur Srivastava (University of Maryland College Park)*

## SESSION 20

Wednesday July 17, 2019

Conference Room 223

### Special Session: Energy-Efficient Machine Learning

Chair: **Caiwen Ding, University of Connecticut**

- 10:00 AM **Deep Learning for Edge Computing: Current Trends, Cross-Layer Optimizations, and Open Research Challenges**  
*Alberto Marchisio (Technische Universität Wien (TU Wien)), Muhammad Abdullah Hanif (Technische Universität Wien (TU Wien)), Faiq Khalid (Technische Universität Wien (TU Wien)), George Plastiras (University of Cyprus (UCY)), Christos Kyrkou (University of Cyprus (UCY)), Theocharis Theocharides (University of Cyprus (UCY)), and Muhammad Shafique (Technische Universität Wien (TU Wien))*
- 10:20 AM **Approximate Computing Applied to Bacterial Genome Recognition using Self-Organizing Maps**  
*Dimitrios Stathis (KTH Royal Institute of Technology, Sweden), Yu Yang (KTH Royal Institute of Technology, Sweden), Saurabh Tewari (IIT Delhi, India), Ahmed Hemani (KTH Royal Institute of Technology, Sweden), Kolin Paul (IIT Delhi, India and TalTech Tallinn University of Technology, Estonia), Manfred Grabherr (Uppsala University, Sweden), and Rafi Ahmad (Inland University of Norway)*
- 10:40 AM **Towards Efficient On-Board Deployment of Deep Neural Networks on Intelligent Autonomous Systems**  
*Alexandros Kouris (Imperial College London, UK), Stylianos I. Venieris (Samsung AI Center, Cambridge, UK), and Christos-Savvas Bouganis (Imperial College London, UK)*

## SESSION 21

Wednesday July 17, 2019

Conference Room 221

### Digital Circuits and FPGA based Designs III

Chair: **Ronald Demara, University of Central Florida**

- 11:00 AM **PVTMC: An All-Digital Sub-Picosecond Timing Measurement Circuit based on Process Variations**  
*Shuo Li (UMass Amherst), Xiaolin Xu (University of Illinois at Chicago), and Wayne Burleson (Umass Amherst)*
- 11:20 AM **Hardware Implementation of Improved Fast-SSC-Flip Decoder for Polar Codes**  
*Jing Zeng (Nanjing University), Yangcan Zhou (Nanjing University), Jun Lin (Nanjing University), and Zhongfeng Wang (Nanjing University)*
- 11:40 AM **A Comparison-free Hardware Sorting Engine**  
*Surajeet Ghosh (Indian Institute of Engineering Science & Technology, India), Shaon Dasgupta (Bentley Systems India Private Limited, Kolkata), and Sanchita Saha Ray (St. Thomas' College of Engineering & Technology, India)*
- 12:00 PM **Adaptive Transceiver for Wireless NoC to Enhance Multicast/Unicast Communication Scenarios**  
*Joel Ortiz Sosa (University of Rennes 1, Inria), Olivier Sentieys (University of Rennes 1, Inria), and Christian Roland (University of Southern Brittany, Lab-STICC)*

## SESSION 22

Wednesday July 17, 2019

Conference Room 223

### Special Session: Botnet of Things: Hardware Insecurity in the IoT Era

Chair: **Jaya Dofe, Florida International University**

- 11:00 AM **Countering Botnet of Things using Blockchain-Based Authenticity Framework**  
*Pinchen Cui (Auburn University) and Ujjwal Guin (Auburn University)*
- 11:20 AM **Aging Analysis of Low Dropout Regulator for Universal Recycled IC Detection**  
*Sreeja Chowdhury (University of Florida), Haoting Shen (University of Florida), Beomsoo Park (University of Florida), Nima Maghari (University of Florida), and Domenic Forte (University of Florida)*
- 11:40 AM **Persistently-Secure Processors: Challenges and Opportunities for Securing Non-Volatile Memories**  
*Amro Awad (University of Central Florida), Suboh Suboh (University of Central Florida), Mao Ye (University of Central Florida), Kazi Abu Zubair (University of Central Florida), and Mazen Al-Wadi (University of Central Florida)*

## SESSION 23

Wednesday July 17, 2019

Conference Room 221

### Digital Circuits and FPGA based Designs IV

Chair: **Nithin Kumar Y. B, NIT Goa**

- 1:00 PM **Focus on What is Needed: Area and Power Efficient FPGAs Using Turn-Restricted Switch Boxes**  
*Fatemeh Serajeh-hassani (Sharif University of Technology), Mohammad Sadrosadati (Sharif University of Technology), Sebastian Pointner (Johannes Kepler University), Robert Wille (Johannes Kepler University), and Hamid Sarbazi-azad (Sharif University of Technology)*
- 1:20 PM **Using Harmonized Parabolic Synthesis to Implement a Single-Precision Floating-Point Square Root Unit**  
*Süleyman Savas (Halmstad University, Sweden), Yassin Atwa (Halmstad University, Sweden), Tomas Nordström (Halmstad University, Sweden), and Zain Ul-Abdin (Halmstad University, Sweden)*
- 1:40 PM **Self Timed SRAM Array with Enhanced Low-Voltage Read and Write Capability**  
*Prasad Vernekar (National Institute of Technology Goa, India), Nithin Kumar Y.B (National Institute of Technology Goa, India), and Vasantha M.H (National Institute of Technology Goa, India)*

## SESSION 24

Wednesday July 17, 2019

Conference Room 223

### Special Session: Secure, Smart, Connected Devices for Emergent Applications

Chair: **Theocharis Theocharides, University of Cyprus**

- 1:00 PM **Towards Hardware-Assisted Security for IoT Systems**  
*Yier Jin (University of Florida)*
- 1:20 PM **Invasive and Non-invasive Analysis of IoT Security**  
*Mohammad Ashiqur Rahman (Florida International University), A. Selcuk Uluagac (Florida International University), Kemal Akkaya (Florida International University)*
- 1:40 PM **Blockchain based distributed key provisioning and Secure Communication over CAN FD**  
*Bryson Shannon (University of North Carolina at Charlotte), Spandana Etikala (University of North Carolina at Charlotte, USA), Yutian Gui (University of North Carolina at Charlotte), Ali Shuja Siddiqui (University of North Carolina at Charlotte), and Fareena Saqib (University of North Carolina at Charlotte, USA)*

## SESSION 25

Wednesday July 17, 2019

Conference Room 221

### Emerging and Post-CMOS Technologies II

Chair: **Ronald Demara, University of Central Florida**

- 2:00 PM **A Hyper-Parameter Based Margin Calculation Algorithm for Single Flux Quantum Logic Cells**  
*Soheil Nazar Shahsavani (University of Southern California) and Massoud Pedram (University of Southern California)*
- 2:20 PM **Ignore Clocking Constraints: An Alternative Physical Design Methodology for Field-coupled Nanotechnologies**  
*Robert Wille (Johannes Kepler University Linz), Marcel Walter (University of Bremen), Frank Sill Torres (DFKI), Daniel Große (University of Bremen), and Rolf Drechsler (DFKI GmbH Bremen)*

## SESSION 26

Wednesday July 17, 2019

Conference Room 223

### System Design and Security IV

Chair: **Chen Liu, Intel**

- 2:00 PM **Mitigating Reverse Engineering Attacks on Deep Neural Networks**  
*Yuntao Liu (University of Maryland, College Park), Dana Dachman-Soled (University of Maryland, College Park), and Ankur Srivastava (University of Maryland, College Park)*
- 2:20 PM **Hardware Watermarking Using Polymorphic Inverter Designs Based On Reconfigurable Nanotechnologies**  
*Shubham Rai (Technische Universitaet Dresden), Ansh Rupani (Technische Universitaet Dresden), Pallab Nath (Indian Institute of Technology Indore), and Akash Kumar (Technische Universitaet Dresden)*
- 2:40 PM **Machine Learning based IoT Edge Node Security Attack and Countermeasures**  
*Vishalini Laguduva (University of South Florida), Sheikh Ariful Islam (University of South Florida), Sathyanarayanan Aakur (University of South Florida), Srinivas Katkoori (University of South Florida), and Robert Karam (University of South Florida)*

\* denotes ISVLSI 2019 Best Paper Nominee